DESIGN OF LOW POWER AND HIGH GAIN BOOSTED OTA FOR HIGH FREQUENCY RADIO MODULATIONS AND TELECOMMUNICATION SYSTEMS

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ABSTRACT

This paper presents the design of high gain and low power fully differential Operational Transconductance Amplifier(OTA). Both the main conventional OTA and the boosting amplifiers are fully differential folded cascode.To increase the open-loop gain of the main OTA two auxiliary operational amplifiers(op-amps) are used . These auxiliary op-amps are fully differential folded cascode op-amps with continuous time Common mode feedbacks (CMFB).CMFB is used in auxiliary op-amps to stablise the designed OTA against temperature. This design has been implemented in 0.18µm CMOS Technology using Cadence EDA tool.Spectre simulation shows that the op-amp has DC gain of 171.7958dB , a noise response of 24.1876nV/Hz, power consumption obtained is 295pW and the unity gain bandwidth is more than 1.5GHz.

KEYWORDS

Boosting amplifiers , Active cascode gain-boosting technique , Fully differential folded cascode , CMFB , Cadence.

1. INTRODUCTION

Nowadays designing high gain and high speed operational amplifier is becoming increasingly challenging because high dc gain characteristics of operational amplifiers demands a multi stage design with long channel devices.In this paper active cascode gain-boosting technique is used along with auxiliary amplifiers to increase the dc gain of an operational amplifier without degrading its high frequency performance.In order to achieve high gain , the single stage amplifier architecture with gain-boosted amplifier will be a nice choice.

To design an analog system, op-amp will be the most important basic building block.Basically an OTA is defined as an op-amp without any output buffer,preventing it from large capacitive loads. Because of their smaller size and simplicity, they are preferred mainly over op-amps. OTA mainly uses differential amplifier at the input and its purpose is to generate a current proportional to an input voltage difference developed at input.

In this paper a gain boosted fully differential OTA is designed to satisfy high gain.The proposed OTA has a **N** gain boost and **P** gain boost auxiliary amplifiers.This auxiliary amplifiers boosts the gain of the main amplifier structure.Section I gives introduction about OTA ansd section II gives information about circuit implementation and section III gives details about simulation results and the finally section IV talks about conclusion of the entire paper.

2.CIRCUIT IMPLEMENTATION

2.1 DESIGN OF THE MAIN AMPLIFIER AND GAIN BOOSTING AMPLIFIER

Gain boosting technology helps in amplifying the op-amps output impedance, thus the overall gain is increased. In order to design high gain designs, two stage configuration might be the appropriate choice. In this paper, two fully differential folded cascode boosting amplifiers has been implemented as shown in Fig.1.And also two compensation capacitors C_C are connected as shown in Fig 1 inorder to achieve desired phase margin.As per the design process , the number of PMOS transistors as are reduced as much as possible because NMOS transistors has 4 times better transconductance compared to the same size PMOS transistors. Two types of CMFBs are used in the design where switched capacitor CMFB circuit is active when the op-amp is in the holding mode and a continuous time CMFB is active when the op-amp is in the sampling mode. The continuous time CMFB circuits are used for the boosting amplifiers.

In this design we have used two types of boosting amplifiers designed with auxillary amplifiers. AN gain boosting amplifier has an NMOS differential input stage, while the AP gain boosting amplifie has a PMOS differential input stage.These auxiliary op amps are used to improve the dc gain of the main op amp.The PMOS type gain boosting amplifier AP is shown in Fig 2 which is similar to the main op amp with the exception that it does not have boosting amplifiers and the input differential stage is of NMOS transistors. The AN boosting amplifier is the same as the PMOS type with the exception that a PMOS differential input stage is used.

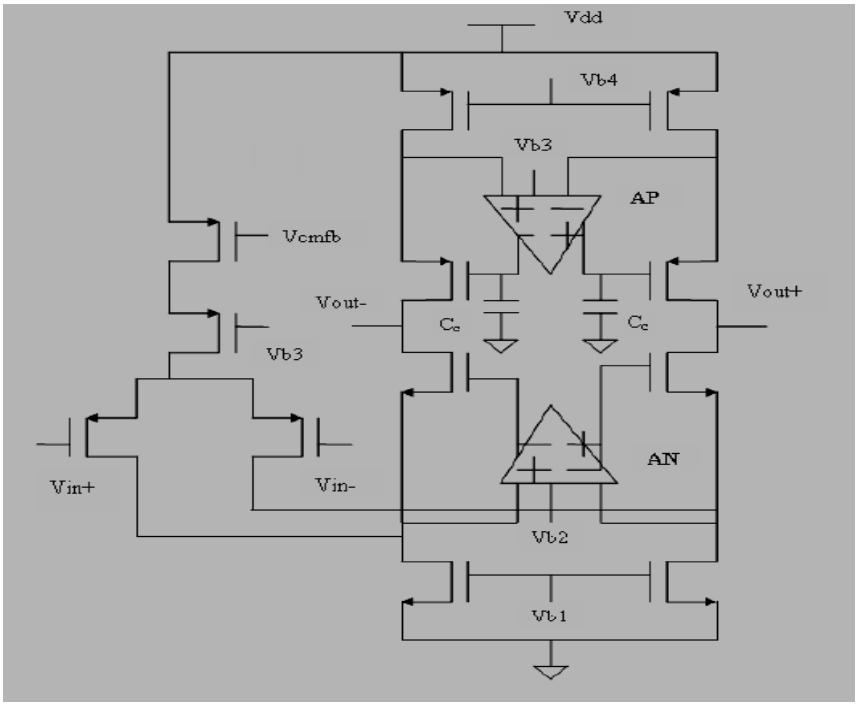

Figure 1 :Fully differential folded cascaded op-amp with fully differential gain-boosted amplifiers.

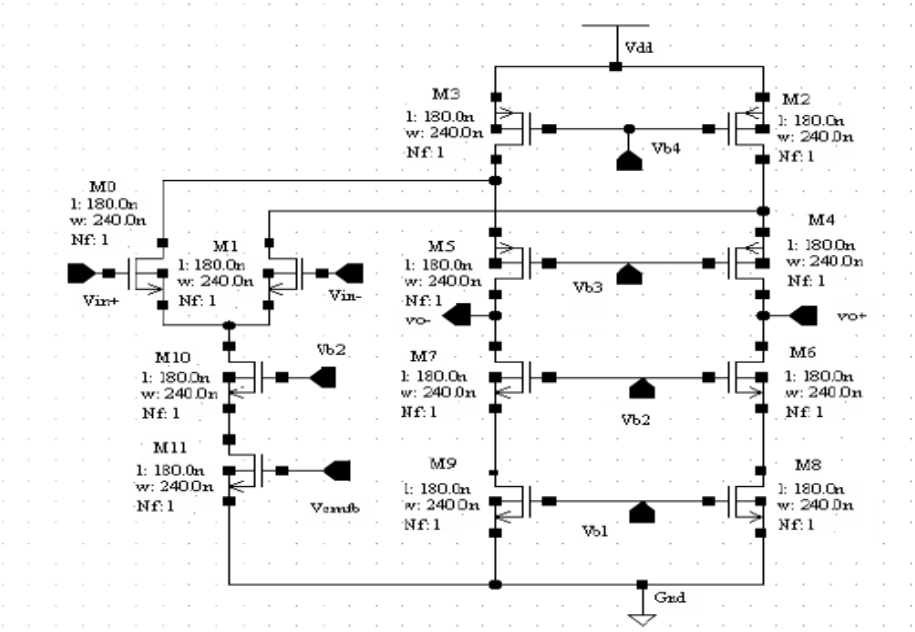

Figure 2:Fully differential gain-boosted amplifier(AP)

2.2 DESIGN OF CMFB CIRCUIT

CMFB is necessary in designing a fully differential OTA to keep the outputs from drifting high or low out of the range where the amplifier provides plenty of gain.The CMFB circuit will enable the op amp to have a common mode output voltage that is immune to variations in the process.CMFB circuit can be divided into:

a.Switched continuous time CMFB(SC-CMFB)
b.Continuous time CMFB circuits.

Generally SCCMFB is preferred because compare to continuous time CMFB ,SCCMFB consumes less power.The SCCMFB is shown in Fig 3.

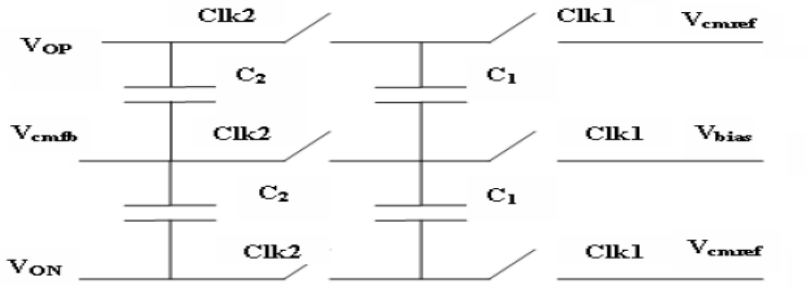

Figure 3:Switched capacitance common mode feedback circuit

The advantage of continuous CMFB circuit is that its speed is fast. Firstly design the boosting amplifier without the CMFB circuit and once it is finished , the CMFB circuit can be used. The CMFB circuit for gain boosting amplifier AP is shown in fig 4.For gain boosting amplifier AN CMFB circuit is similar to the AP except that the input differential pair is of NMOS transistors.For main op amp and boosting amplifiers bias voltages will enable those transistors to work in saturation region.

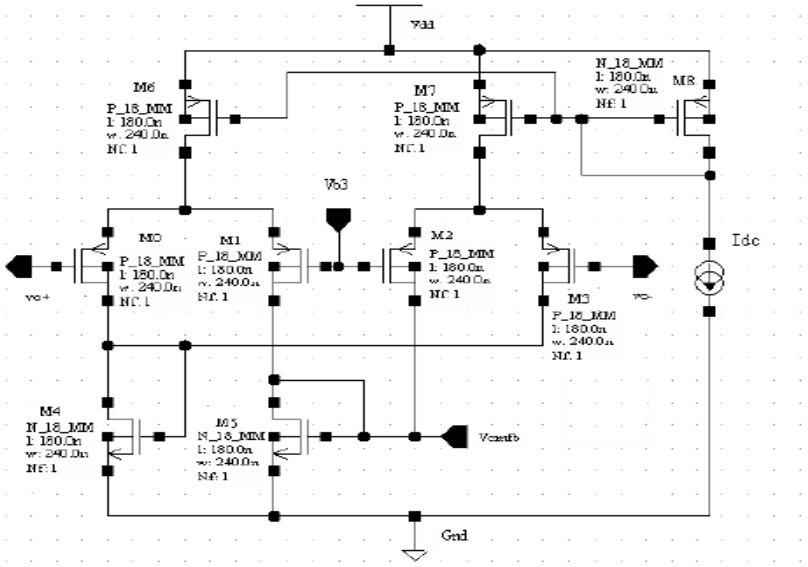

Fig 4:CMFB circuit for gain boosting amplifier AP.

3.SIMULATION RESULTS

A single stage fully differential gain boosted folded cascode op-amp is designed with the design process described above and implemented in 0.18µm process with 1.8 V power supply and simulated with Cadence spectre EDA tool.The load capacitance is taken as 1 pF. The simulation results obtained are shown in table 1.

PARAMETER	VALUES
Technology	180nm
UGB	More than 1.5GHz
C_L	1pF
Noise	24.186nV/Hz
Gain	171.7958dB
Power	295.567pW
Supply Voltage	1.8V

Table 1:Simulation results

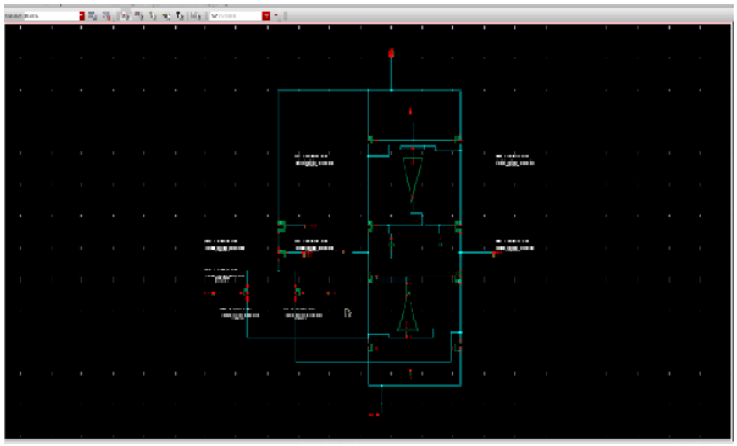

Figure 5:Gain boosted OTA design in cadence

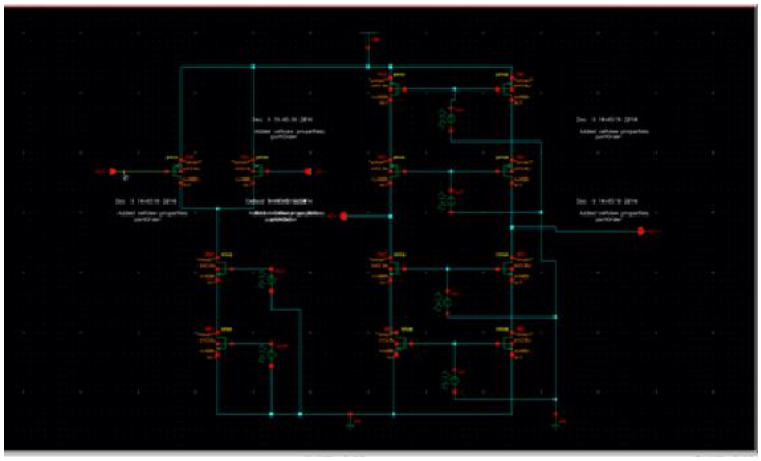

Figure 6:AN schematic

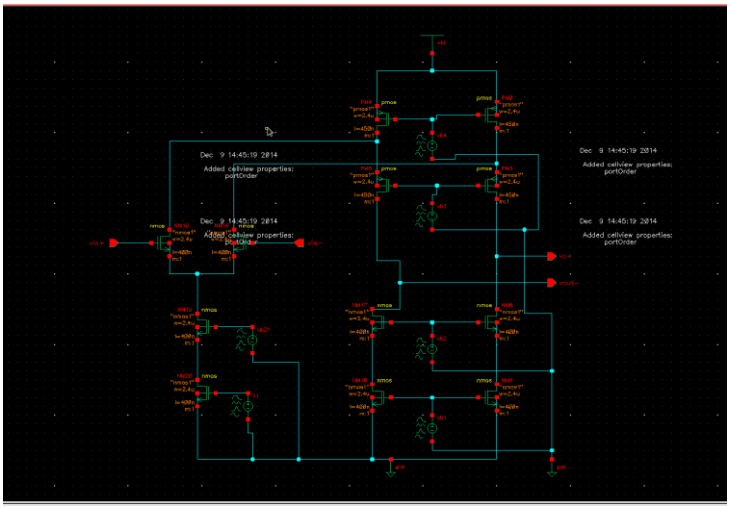

Figure 7:AP schematic

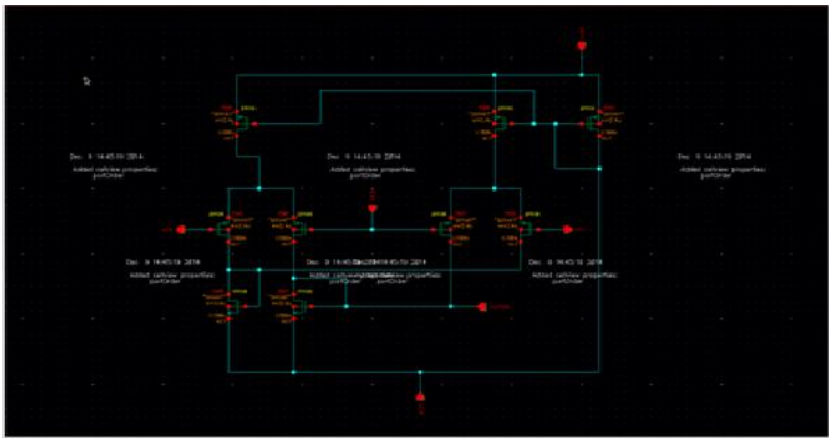

Figure 8:CMFB circuit schematic

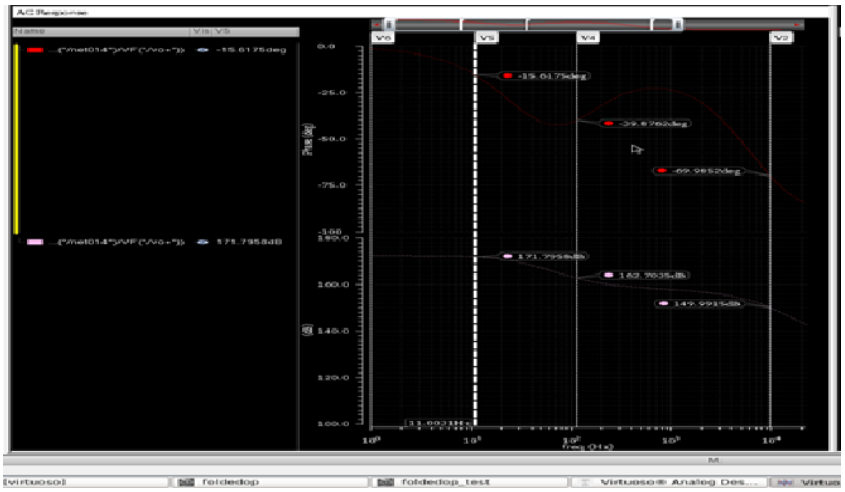

Figure 9:Phase and Gain

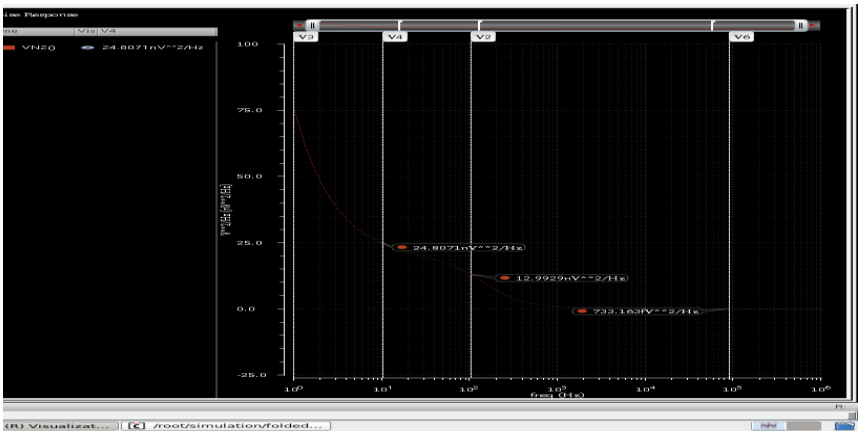

Figure 10:Noise response

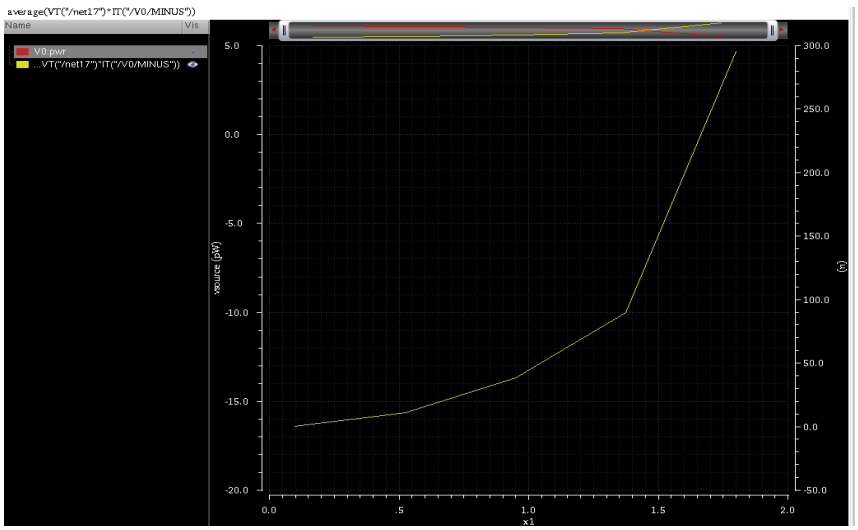

Figure 11:Power output

4.CONCLUSION

The design and experimental results of a fully differential amplifier with gain boosting technology is been presented. Using 0.18µm CMOS process, it is noted that design has good performance with a dc gain of 171.7958dB, noise response of 24.186nV/Hz, power consumption of 295.567pW and a UGB is more than 1.5GHz at a power supply of 1.8V. This designed Gain-Boosted OTA is very well used for High Frequency Radio Modulations and Telecommunication Systems frequency range.

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REFERENCES

[1] B. Razavi, Design of analog cmos integrated circuits (Tata McGraw-Hill Edition, 2002).

[2] R. J. Baker, H. W. Li and D. E. Boyce, CMOS circuit design, layout and simulation (IEEE, Press Series on Microelectronic Systems, Prentice Hall of India Private Limited,2004).

[3] D. Flandre etc., Improved synthesis of gain-boosted regulated cascode cmos stages using symbolic analysis and gm/Id methodology, IEEE Journal of Solid-State Circuits, Vol. 32, No. 7, 1997, 1006-1012.

[4] M. Das, Improved Design Criteria of Gain-Boosted CMOS OTA with High-Speed Optimizations, IEEE Trans. on Circuits and Systems II Vol. 49, No. 3, 2002, 204-207.

[5] D. Johns and K. Martin, Analog integrated circuit design, 287, 1997.

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