Development of Improved Diode Clamped Multilevel Inverter Using Optimized Selective Harmonic Elimination Technique

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ABSTRACT

In this paper the role of Selective Harmonic Elimination (SHE) is presented for diode clamped twelve-level multilevel inverter (DCMLI) based on dog leg optimization algorithm. Non-linear equations has been solved to eliminate specific low order harmonics, using the developed DOP algorithm, while at the same time the fundamental component is retained efficiently. The non-linear nature of transcendental equation provide multiple or even no solution for a particular modulation index. The proposed optimization method solving the nonlinear transcendental equations providing all possible solutions. The paper also showing the comparison between different modulation techniques including the proposed method. The entire system has been simulated using MATLAB/Simulink. Simulation results confirm the effectiveness with negligible THD.

KEYWORDS

DCMLI,SHEPWM, Switching Angles, DOP, THD

I. INTRODUTION

In power electronics, the development of multilevel inverter provide a new and alternative option in high power applications. The high voltage sharing ability, low electromagnetic interference (EMI), lower harmonics, made multilevel inverter a very hot area in today's power system and large motor drives. It is not difficult to develop high voltage inverters with multilevel structure in which voltage are controlled, but the main problem is the harmonic distortion in the output waveform. Recently many modulation techniques such as SPWM, SVPWM, SHEPWM, etc[1] have been used to address this problem. SHEPWM technique can lower the harmonic content of the output current as well as resonant harmonic. In the same manner different types of multilevel are used for the purpose of reduction in harmonics and improvement in power quality[2]. Cascaded five level multilevel inverter using DSTATCOM implemented for power improvement[3].Chopper with flying capacitor used in DCMLI for the reduction of stress and produces AC voltage[4]. The paper[5] presents voltage sharing for high power factor loads based on DCMLI(4-levels). SVPWM based[6] 3-level diode clamped multilevel level inverter is presented for leakage current in PV system. 3-level DCMLI with ANPC, ZCT used for sustainable energy[7].Building H-Bridge for AC to DC conversion with the use of capacitors and

single DC source with less harmonics[8]. Using different voltage balancing equations and techniques to form a flying capacitor H-Bridge multilevel inverter[9].Cascaded inverters with particle swarm optimization technique to improve power quality and reduce total harmonics[10].Cascaded inverter using SVPWM to minimize harmonics and switching frequency[11].Many multi -level inverters are used but diode clamped multi-level inverter (DCMLI) is employed for many applications like power drives & utility system [12].

In this proposed method diode clamped 12 level inverter is implemented using selective harmonic elimination pulse width modulation technique (SHEPWM) to reduce the total harmonic distortion of the output wave form and improve quality of power. Optimization technique dog leg is used for switching angles of IGBTs employed in the system and the switching angles are solved by non-linear transcendental equations which contain trigonometric terms. Newton-Repshan is used to solve thesetranscendental equations.

II. WORKING PRINCIPLE

The basic working principle block diagram of SHE was shown in Figure 1. Table 1 showsthe number of on and off switches for different levels of output voltage in a half cycle (0to90^{o}) for 12levels DCMLI's. At any level number of on switches = (m/2)-1 while each switch is turned on once at a time.

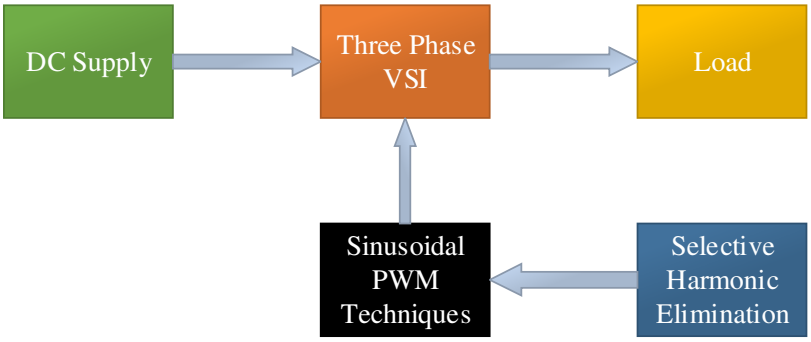


Figure 1 Block Diagram of Selective Harmonic Elimination

The output of DCMLI is a stepped waveforms shown in Figure 2 for each step IGBT is switched at an angle such that the total harmonic distortion is reduced. To get a desired value of fundamental component of voltage and reduced THD, Selective harmonic elimination PWM method is used. Selective Harmonic elimination (SHEPWM) is used for low switching frequency and removing lower order odd harmonics such as 3rd, 5th, 7th, 11th and 13th. This method further uses of iterative optimization technique 'trust region dogleg' algorithms to compute switching angles (α).

Table 1IGBTs Switching Pattern for 12 DCMLI

Stepped Voltages	Conducting Switches	Non Conducting Switches
0Vdc	12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33	1 2 3 4 5 6 7 8 9 10 11 34 35 36 37 38 39 40 41 42 43 44
1Vdc	11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32	1 2 3 4 5 6 7 8 9 10 33 34 35 36 37 38 39 40 41 42 43 44
. . .	. . .	. . .
10Vdc	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23	1 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
11Vdc	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22	23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44

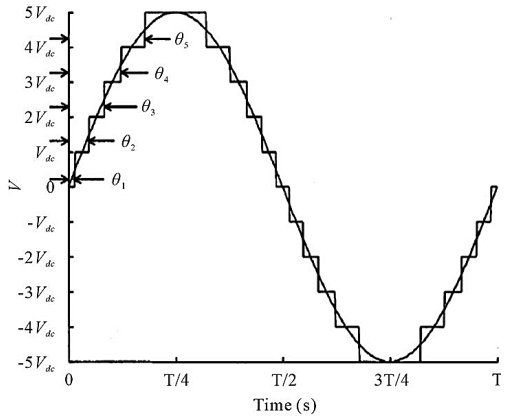


Figure 2: Stepped Diode Clamped Multi Level Inverter Output

III. CALCULATION FOR DOG LEG ALGORITHM

Equations of the output voltage of DCMLI, peak values of harmonics for the calculation of THD and the system of non- linear equations for switching angles calculation are derived from Fourier series. Fourier series for a periodic function is expressed in (1)

$$f_t = a_v + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_o t) + b_n \sin(2\pi n f_o t) \quad (1)$$

Here a_v , a_n and b_n are the Fourier series coefficients and f_o is the fundamental frequency. (2), (3) & (4) shows relationships to determine the values of these coefficients

$$a_v = \frac{1}{T} \int_{t_o}^{t_o+T} f(t)dt \quad (2)$$

$$a_n = \frac{2}{T}\int_{t_o}^{t_o+T} f(t)\cos(2\pi n f_o t)dt \tag{3}$$

$$b_n = \frac{2}{T}\int_{t_o}^{t_o+T} f(t)\sin(2\pi n f_o t)dt \tag{4}$$

Where t_o = Chosen time reference, T = Fundamental period.
For a signal having odd quarter wave Symmetry, Fourier series coefficients are given as

$$a_v = 0 \qquad a_n = 0 \quad for\ all\ n \qquad b_n = 0 \quad for\ n\ even$$

And

$$b_n = \frac{8}{T}\int_0^{T/4} f(t)\sin(2\pi n f_o t)dt \qquad for\ odd\ n \tag{5}$$

The Multilevel inverter has odd quarter wave symmetry. Using Fourier coefficient equations of a quarter waves, Fourier coefficients for a DCMLI output are derived in terms of switching angles. Five angles are considered here only for mathematical calculations.

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} f(\frac{\omega t}{2\pi f_o})\sin(n\omega t)d(\omega t) \qquad for\ n\ odd \tag{6}$$

$$b_n = \int_{\alpha_1}^{\alpha_2}\frac{4}{\pi}(v_{dc})\sin(n\omega t)d(\omega t) + \int_{\alpha_2}^{\alpha_3}\frac{4}{\pi}(2v_{dc})\sin(n\omega t)d(\omega t) + \int_{\alpha_3}^{\alpha_4}\frac{4}{\pi}(3v_{dc})\sin(n\omega t)d(\omega t) + \int_{\alpha_4}^{\alpha_5}\frac{4}{\pi}(4v_{dc})\sin(n\omega t)d(\omega t)$$
$$+ \int_{\alpha_5}^{\pi/2}\frac{4}{\pi}(5v_{dc})\sin(n\omega t)d(\omega t) \tag{7}$$

where $\alpha_1, \alpha_2, \alpha_3, \alpha_4$ and α_5 are the switching angles

Solving Integration results

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} f(\frac{\omega t}{2\pi f_o})\sin(n\omega t)d(\omega t) \qquad for\ n\ odd$$
$$b_n = -\frac{4}{\pi n}v_{dc}\left[\cos(n\omega t)\right]_{\alpha_1}^{\alpha_2} - \frac{4}{\pi n}(2v_{dc})\left[\cos(n\omega t)\right]_{\alpha_2}^{\alpha_3}$$
$$-\frac{4}{\pi n}(3v_{dc})\left[\cos(n\omega t)\right]_{\alpha_3}^{\alpha_4} - \frac{4}{\pi n}(4v_{dc})\left[\cos(n\omega t)\right]_{\alpha_4}^{\alpha_5}$$
$$-\frac{4}{\pi n}(5v_{dc})\left[\cos(n\omega t)\right]_{\alpha_1}^{\alpha_2} - \frac{4}{\pi n}(2v_{dc})\left[\cos(n\omega t)\right]_{\alpha_5}^{\alpha_{\pi/2}} \tag{8}$$

$$= \frac{4}{\pi n} v_{dc} \left[\cos(n\alpha_1) - \cos(n\alpha_2)\right] + \frac{4}{\pi n}(2v_{dc})\left[\cos(n\alpha_2) - \cos(n\alpha_3)\right]$$
$$+ \frac{4}{\pi n}(3v_{dc})\left[\cos(n\alpha_3) - \cos(n\alpha_4)\right] + \frac{4}{\pi n}(3v_{dc})\left[\cos(n\alpha_4) - \cos(n\alpha_5)\right] \quad (9)$$

Where n is an odd integer

$$\cos\left(n\frac{\pi}{2}\right) = 0 \ , \ b_n = \frac{4}{\pi n} v_{dc}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) + \cos(n\alpha_5)\right] \quad (10)$$

(10)provides peak values of odd harmonics in a DCMLI which can be used to calculate total harmonic distortion (THD) using(11).

$$THD = \frac{\sqrt{v_2^{\,2} + v_3^{\,2} + v_4^{\,2} \ldots . v_n^{\,2}}}{v_1} \qquad v_1, v_2, v_3 \ldots . v_n \ \textit{are the peak values of harmonics} \quad (11)$$

Using resultant theory, a set of non- linear equations is derived from(10)which can is solved for the values of angles. In case of twenty fourlevelsDCMLI, following set of equations is obtained to eliminate odd harmonics upto eleventh level.

$$\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \ldots\ldots \cos(3\alpha_{11}) = 0 \quad (12)$$

$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \ldots\ldots \cos(7\alpha_{11}) = 0 \quad (13)$$

$$\cos(9\alpha_1) + \cos(9\alpha_2) + \cos(9\alpha_3) + \ldots\ldots . \cos(\alpha_{11}) = 0 \quad (14)$$

$$\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) \ldots . + \cos(11\alpha_{11}) = 0 \quad (15)$$

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \ldots\ldots \cos(\alpha_{11}) = \frac{mM\pi}{4} \quad (16)$$

$$M = \frac{v_1}{v} \quad (17)$$

m=(number of levels/2)-1

Switching angles are calculated with the help of MATLAB program using trust region dogleg algorithm (shown in fig) for a range of modulation indexes. Table 2 angles are calculated using (18) is satisfied.

$$\{0 \le \alpha_1 \le \alpha_2 \le \alpha_3 \le \alpha_4 \le \alpha_5 \le \alpha_6 \le \alpha_7 \le \alpha_8 \le \alpha_9 \le \alpha_{10} \le \alpha_{11}) \quad (18)$$

Where α is an array containing initial guess for $\alpha_1 + \alpha_2 + \ldots\ldots \alpha_n$

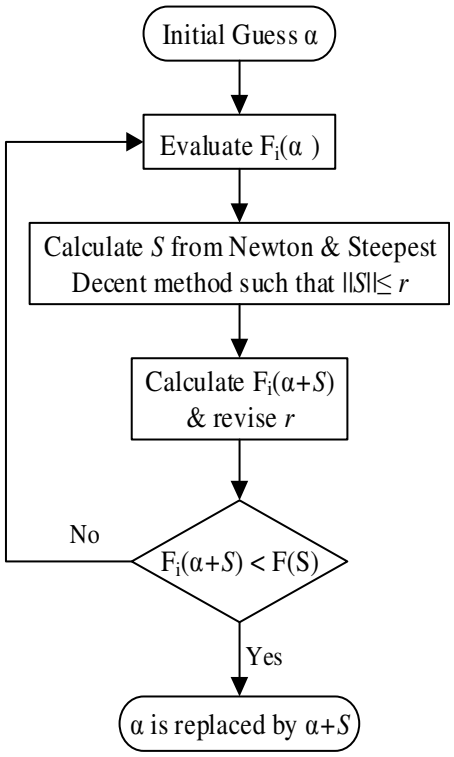


Figure 3: Proposed Dog Leg Algorithm

$$F(\alpha) = \sum_{i=1}^{n} [F_i(\alpha)]^2 \tag{19}$$

S is correction step and r is radius of trust region. Figure 4 shows the proposed flow chart of trust region dogleg method for computing $\alpha_1 + \alpha_2 + ...\alpha_n$ from set of functions $f_1, f_2, f_3.....f_n$

In first step, a correction step is calculated which is added to the initial guess. Dogleg utilizes Newton and steepest descent methods. The combination of these two methods ensures a fast convergence and a solution of function in the steepest descent direction. The second step involves finding the value of trust region radius to estimate length of step for the current iteration such that the following condition is obeyed.

$$F(\alpha + s) < F(\alpha) \tag{20}$$

Third step performs a check the new values of function. Has the function minimized.

Table 2: Optimized switching angles in radians for 12 level DCMLI

M	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}	α_{11}
0.95	0.0541	0.1463	0.2461	0.3331	0.4356	0.5740	0.6757	0.7713	0.9824	1.1195	1.5009
0.9	0.0000	0.1502	0.2408	0.3593	0.4916	0.6036	0.7106	0.8380	1.0304	1.3253	1.5308
0.85	0.0000	0.1731	0.2623	0.4003	0.4934	0.6137	0.8056	0.8958	1.1659	1.4188	1.6604
0.8	0.0000	0.1694	0.3155	0.3906	0.5308	0.6896	0.8212	1.0237	1.2916	1.4870	1.5708
0.75	0.0000	0.1870	0.3287	0.4196	0.5761	0.7428	0.8929	1.1568	1.4078	1.5424	1.57
0.7	0.0000	0.2499	0.2826	0.4834	0.6322	0.7779	0.0296	1.2290	1.4645	1.5617	1.5700

IV. IMPLEMENTATION OF 12 LEVEL DCMLI USING SHEPWM

12 level diode clamped multilevel inverter (DCMLI) with four sub-systems connected to DC batteries sources and switches state controller (SSC) is shown in fig.01.it consists of specific number of diodes, switches (IGBT's) and DC sources. The components required are calculated using equations 1, 2, 3.

Number of IGBTs = $4\left[(m/2)-1\right]$ (21)

Number of IGBTs =44

Number of clamping diodes=$\{(m/2)-1\}*\{(m/2)-2\}$ (22)

Number of clamping diodes =110

Number of batteries=$(m/2)-1$ (23)

Number of batteries =11

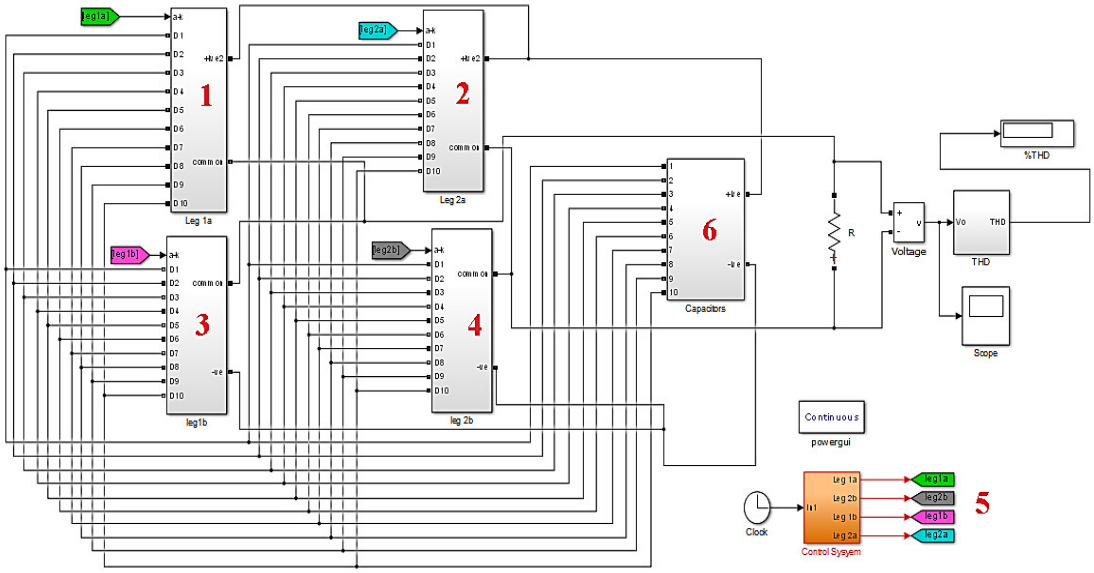
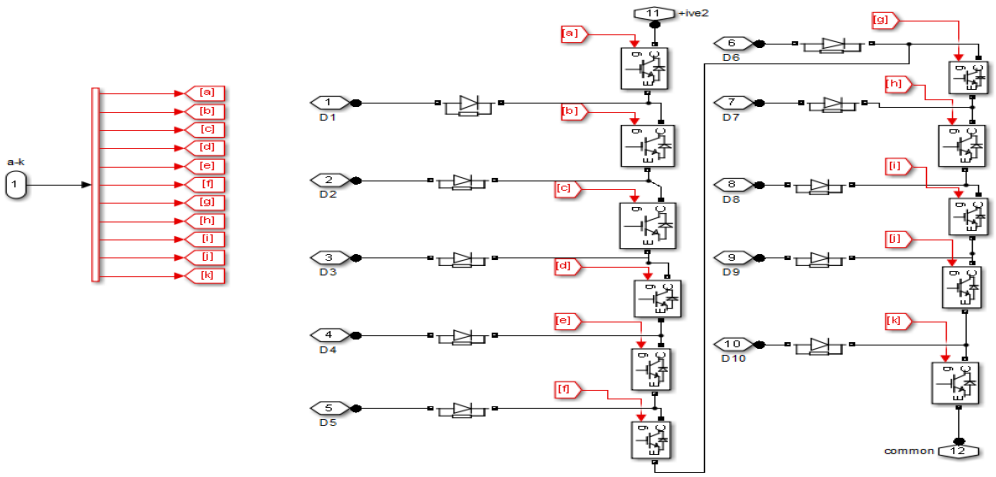


Figure 4: 12 Levels DCMLI

Figure 4 shows the overall system of DCMLI. In figure,1 & 3 shows the first leg of positive terminal of output DC similarly 2 & 4 shows the 2nd leg of negative terminal of output DC. 5 generates the control signals to legs and 6 contains the number of capacitors for multilevel arrangement. Figure5 shows Leg 1a of 12 levels DCMLI which is connected in series with leg1b to complete first leg as there are two legs in this system. Second leg is similar to first leg. Both first and second legs are connected to form a full H-Bridge DCMLI.



V. SIMULATION RESULTS

Experimental results are obtained for optimized switching angles using dog leg method and for non-optimized IGBTs switching angles. Experimental results include shows

- Values of total harmonic distortion
- Harmonic order of harmonics with reference to fundamental component
- Effect of modulation index on THD.

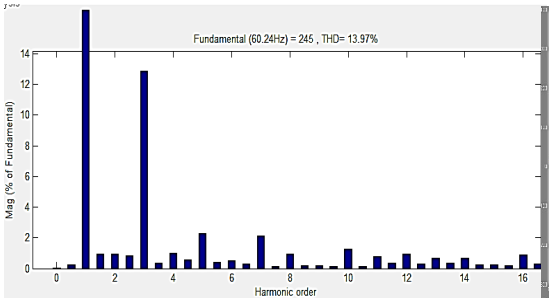


Figure 6: THD and Frequency spectrum of 12 Level DCMLI non- optimized and m=0.95

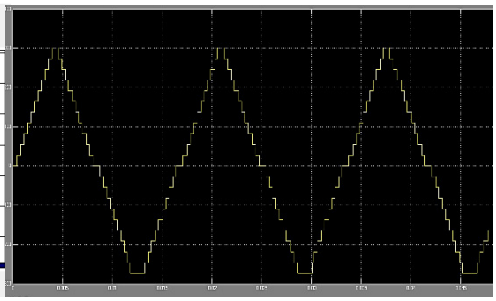


Figure 7: Voltage Waveform of 12 levels DCMLI with non-optimized angles

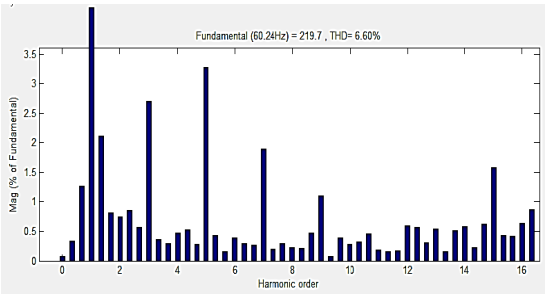


Figure 8: THD and Frequency spectrum of 12level DCMLI with optimized angles

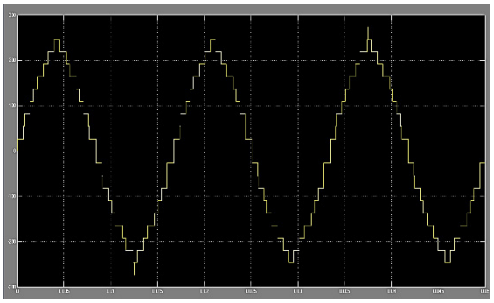


Figure 9: Voltage Waveform of 12 Level DCMLI levels optimized and m =0.7

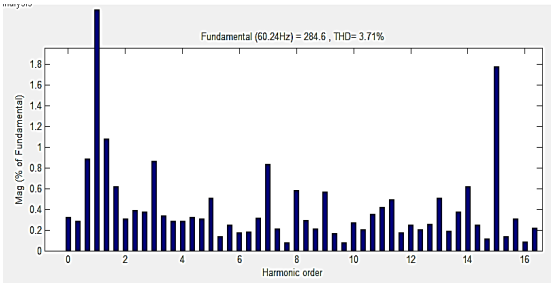


Figure10: THD and Frequency spectrum of 12 level DCMLI DCMLI with optimized angles (m=0.95)

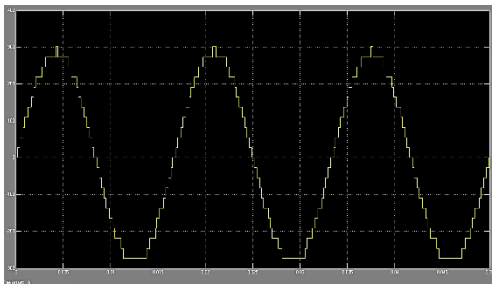


Figure 11:Voltage Waveform of 12 Level optimized and m =0.95

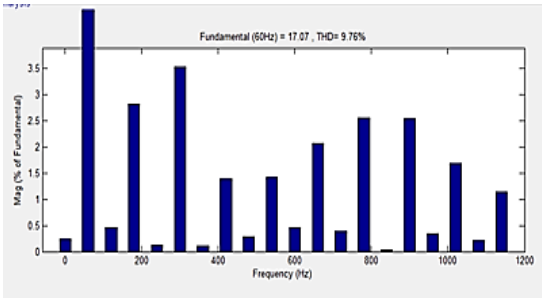


Figure 12: THD and Frequency spectrum of 5-levels DCMLI with optimized angles (m=0.95)

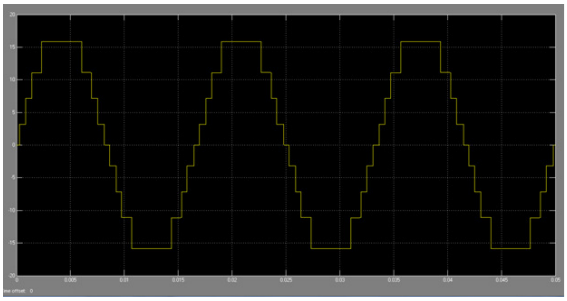


Figure 13:Voltage Waveform of 5- Level DCMLI optimized and m=0.95

Table 3 shows the THD at different modulation indexes and Figure 14 show that the THD will decrease as modulation index increases.

M	THD
0.95	3.80
0.9	4.80
0.85	5.65
0.8	5.80
0.75	6.12
0.7	6.49

Table 3:THD at different Modulation index

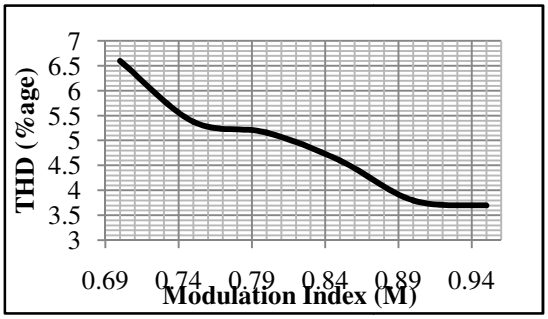


Figure 14:Comparison of THD vs Modulation Index

Table 4 shows a comparison of various techniques employed for 5-level diode clamped inverter to reduce total harmonic distortion(THD).modulation techniques like POD-PWM, SPWM, Third harmonic injection, offset voltage and trapezoidal are used but proposed technique in this paper improves output voltage waveform with lowest THD value and power factor value near to 1.

No.	Modulation Technique	%THD
1	POD-PWM[12]	32.32
2	Trapezoidal[13]	18.39
3	Three harmonic Injection[14]	17.57
4	Third harmonic injection[13]	17.03
5	SPWM[13]	16.97
6	SPWM[15]	16.82
7	Offset voltage[13]	16.38
8	Proposed Technique (SHEPWM)With Dog Leg Method	9.76

Table 4: THD values of 5-level multilevel diode clamped inverters using different modulations techniques

VI. CONCLUSION

In this paper, SHEPWM strategy is taken under consideration for elimination of desired low order harmonics. The corresponding switches angles for DCMLI is calculated using dog leg

optimization algorithm. Undesired harmonics are eliminated to possible maximum limits and the fundamental voltage is maintained at desired level, thus resulting the minimum THD. The proposed technique can be applied to any multilevel inverter configurations and we can generalize this method to any higher order inverters.

REFERENCES

[1] Peddapeli.S.K, (2014) "Recent Advances in Pulse Width Modulation Techniques andMultilevel Inverters"International Journal of Electrical, Electronic Science and EngineeringVol 8 No 3, pp-568-576.

[2] Hussein. H, (2014) "Harmonics Elimination PWM (HEPWM)" International Journal of Engineering Research and General Science Vol 2, No 2, pp-172-181.

[3] Satyanarayana, G. V. R., & Ganesh, S. N. V, (April 2010)"Cascaded 5-level inverter typeDSTATCOM for power quality improvement"InStudents' Technology Symposium (TechSym), 2010 IEEE (pp. 166-170).

[4] Shukla, A., Ghosh, A., & Joshi, A, (2010) "Flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter" Industrial Electronics, IEEE Transactions on, 57(7), pp2249-2261.

[5] Boora, A. A., Nami, A., Zare, F., Ghosh, A., &Blaabjerg, F, (2010) "Voltage-sharing converter to supply single-phase asymmetrical four-level diode-clamped inverter with high power factor loads"Power Electronics, IEEE Transactions on, 25(10), pp2507-2520.

[6] Cavalcanti, M. C., Farias, A. M., Oliveira, K. C., Neves, F. A., &Afonso, J. L, (2012)"Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems" Industrial Electronics, IEEE Transactions on, 59(1), pp435-443.

[7] Li, J., Liu, J., Boroyevich, D., Mattavelli, P., &Xue, Y, (May, 2011) "Comparative analysis of three-level diode neural-point-clamped and active neural-point-clamped zero-current-transition inverters" In Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference (pp. 2290-2295)

[8] Du, Z., Tolbert, L. M., Ozpineci, B., &Chiasson, J. N, (2009) "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter" Power Electronics, IEEE Transactions on, 24(1), pp25-33.

[9] Khazraei, M., Sepahvand, H., Corzine, K. A., &Ferdowsi, M, (2012) "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters".Industrial Electronics, IEEE Transactions on, 59(2), pp769-778.

[10] Rodriguez, J. C., & P Moran, L, (2001) "A vector control technique for medium voltage multilevel inverters" Applied Power Electronics Conference and Exposition, 2001.APEC 2001.

[11] J. Rodriguez, J. S. Lai, and F. Z. Peng, (2002) "Multilevel inverters: A survey of topologies, controls, and applications" IEEE Trans. Ind. Electron., Vol.49, no. 4, pp. 724–738.

[12] Chaturvedi. R,(2014) "A Single Phase Diode Clamped Multilevel Inverter and its Switching Function". Journal of Innovative trends in Science, Pharmacy & Technology. Vol-1(1),pp.63-66.

[13] Haskar Reddy, V. N.,Babu, C. S. & Suresh, K, (2011) "Advanced Modulating Techniques for Diode Clamped Multilevel Inverter Fed Induction Motor"Vol. 6, No 1,pp. 90-99.

[14] Zheng, X., Song, L., & Hongying, P, "Study of Five-level diodes-clamped Inverter Modulation Technology Based on Three-harmonic Injection Method" 2nd International Conference on Electronic & Mechanical Engineering and Information Technology 2012.

[15] Kedareswar.M., (2013) "Reduction of THD in Diode Clamped Multilevel Inverter employing SPWM technique"International Journal of Scientific and Research Publications, Vol 3, No 6, pp.1-4.

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