

# ANALYSIS OF ELECTROMAGNETIC COUPLING BETWEEN TWO NON-PARALLEL MICROSTRIP LINES ON A HIGH SPEED PRINTED CIRCUIT BOARD

M.Anandan<sup>1</sup>, Dr.N.Suresh Kumar<sup>2</sup>, P.Rajeswari<sup>2</sup>, A.Gobinath<sup>2</sup>

<sup>1</sup>Department of Electronics and Communication Engineering, Latha Mathavan Engineerign College, Madurai.

<sup>2</sup>Velammal College of Engineering and Technology, Madurai

## ABSTRACT

*Coupling among interconnects and PCB traces is a major limiting factor of signal quality in high speed digital system. This paper evaluates a possible way of far-end coupling reduction in a special geometry of traces. In this work, via stitch guard is constructed between the non-parallel microstrip lines to control the coupling. In a practical high speed printed circuit board, coupling between non-parallel traces is common. The effects of via stitch guard for alleviating the coupling are investigated. The coupling is controlled by adjusting the inclination of any one of the line. The results are compared with conventional traces. Some design guidelines for proper inclination angle of line for reducing the far-end coupling are concluded.*

## KEYWORDS

*Coupling, Non-parallel microstriplines, Via stitch guard, Inclination*

## 1. INTRODUCTION

Due to the advancements in electronic packaging technology, a new paradigm of electronic system design has emerged to compactly integrate multi-functional electronic circuits. Further component and packaging miniaturization has resulted in dense routing topologies, which are prone to signal integrity problems. Signal integrity or SI is a set of measures of the quality of an electrical signal. Some of the main issues of concern for signal integrity are ringing, coupling, ground bounce, distortion, signal loss and power supply noise. Signal integrity is an important factor in the design of high speed PCB. At this level, interconnects become more vulnerable to signal integrity problems. So designing an interconnect in a proper way to avoid this signal integrity problem is a main issue. Generally coupling is ignored for relative low frequency circuits, become critical for reliable circuit operation and the success of the overall system performance. The far-end coupling coupling is of particular interest due to the significantly stronger coupling as compared to that at the near end. To alleviate the coupling of coupling between transmission lines various methods have been established. One way to reduce the far-end coupling in the parallel microstrip lines, the extra dielectric material can be deposited over the microstrip lines. This material deposition is a cost adding process. Another way to reduce

coupling is widening the space between two lines. This method may occupy more space and thus reduce the routing flexibility. Therefore, it is not suitable for non-parallel lines. Traditionally, guard traces are used to control the coupling between two parallel microstrip lines. Another solution is to place metal vias or plated holes between the adjacent lines to reduce the coupling between them. Via holes are easy and inexpensive to build using the current fabrication process for the commonly used PCBs. In PCB or IC layout, coupling lines may be placed at different angles with regard to each other in the adjacent layers or even in the same layer. To this end, this paper introduces new method to reduce far-end coupling between two non-parallel traces on a high speed printed circuit board. Here we have studied the use of via stitch guard trace for non-parallel lines. The results are compared with the conventional configuration and also find the optimum angle between two non parallel lines for minimum coupling.

## 2.Non-Parallel Microstrip Lines

Microstrip lines are widely used for the high- speed signal interface on printed circuit boards mainly used for low cost. Microstrip lines do not support pure TEM modes, but at low frequencies they support quasi-TEM modes that approximately satisfy the transmission line equations. Fig.1 shows a pair of microstriplines on a grounded substrate.

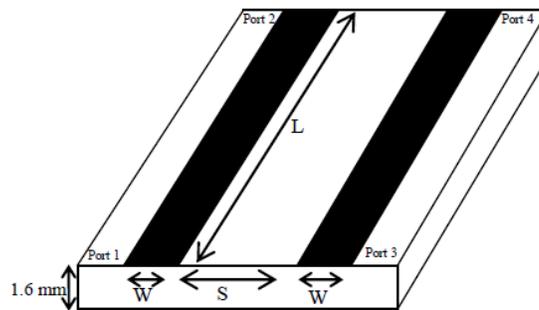


Figure.1. PCB Structure With Two Microstrip lines

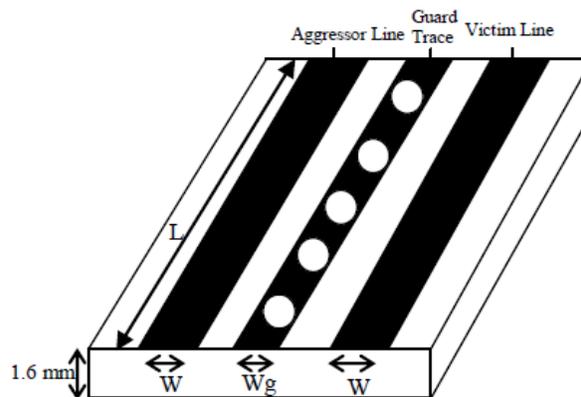


Figure.2. Guard Trace and Grounded Vias

For simplicity, we assume that the two strips have equal width  $W$ , zero thickness, and perfect conductivity. The ground plane is also assumed to be perfectly conducting. The lines are located on a dielectric substrate thickness  $h$  and have a separation  $S$ . The substrate has relative permittivity  $\epsilon_r$ . Fig.2 shows the structure of two parallel lines with via-stitch guard trace. One way to reduce the coupling without enlarging the distance between two lines is to insert guard trace between the aggressor and victim lines. A guard trace, which is a kind of shield line, can be used to reduce the coupling between the aggressor and victim lines [4]. A grounded shield line is known to be effective to reduce the capacitive coupling of on chip interconnects. However, the conventional guard trace is not effective to reduce the coupling of transmission lines on PCB. The reason is that the guard trace cannot maintain the ground potential at all the positions along the trace because the guard trace itself is a transmission line.

As illustrated in Fig 2, a guard trace is usually introduced between line1 and line2. Here, we assume that the guard trace is 1 mm wide; the length of guard trace is same as that of line 1 and 2. It is terminated at both ends by the matched impedance 50 ohms.

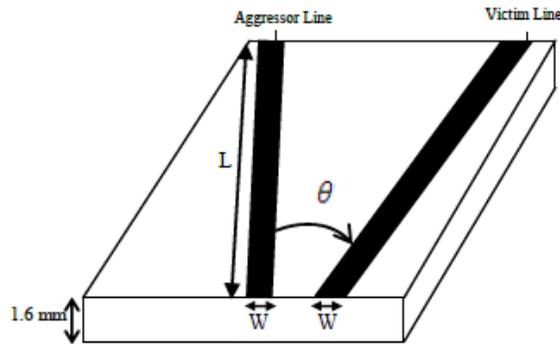


Figure.3. Non Parallel Microstrip lines

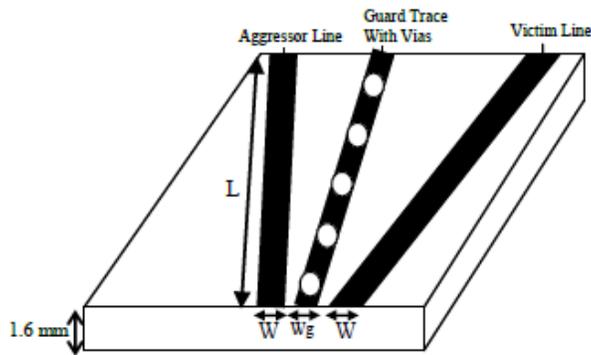


Figure.4. Non-Parallel Microstrip lines with Via Fence

The model considered in this work is shown in Fig.3. Two non parallel microstrip lines of the same dimensions, length( $L$ ) 100mm, width 3mm are etched on the substrate of thickness 1.6mm and relative permittivity of 4.4. The near-end ports of two lines are with a separation of 13.5 mm

and far-end ports of two lines are with a separation of 64.96 mm. Fig.4 shows the non-parallel microstrip line with via stitched guard trace. The length and width of the microstriplines are similar to physical dimensions of Fig.3. The vias are uniformly distributed with the spacing of  $G$  is 30mm. The diameter of via is chosen as 1mm.

### 3. Simulation results

In simulation experiments, our research is focused on how to reduce the coupling between a pair of transmission lines on a printed circuit board. In this simulation, the structure of parallel and non-parallel transmission line can be treated as a symmetrical four port networks. Port 1 is input port, then port 3 is the cutoff port, port 4 is the coupling port. Because of the symmetry,  $S_{14}=S_{41}$ , so  $S_{41}$  is the main parameter for analyzing coupling between a pair of transmission lines. Each port is matched with a resistance of  $50 \Omega$ . The thickness of the PCB is 1.6 mm and the relative dielectric constant of the medium is 4.4. The sweep frequency is from 0 to 6 GHz. The Sweep step is 100MHz. The conventional and proposed structures were simulated using Agilent Advanced Design System (ADS) to calculate the far-end coupling ( $S_{41}$ ) over a frequency range from 0 to 6 GHz. The simulation method is the momentum method, the grids are set interms of 30 grids/  $\lambda$  ( $\lambda$  is the wavelength of the signal whose frequency is 6 GHz). Here, we present a comparison of the calculated results. From Fig4 – Fig 12 shows the simulated results of near-end and far-end coupling for conventional structures and proposed structure for coupling reduction.

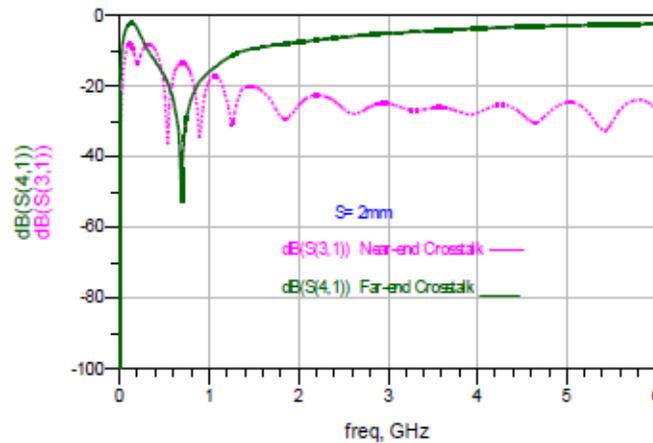


Figure.5. Simulation Results of Near and Far end Coupling for Parallel Microstrip lines in spacing  $S=2$  mm

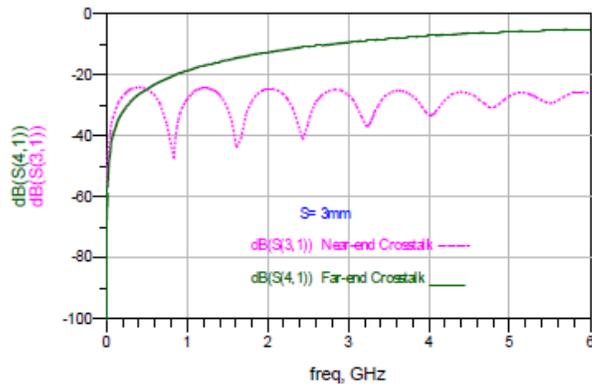


Figure.6. Simulation Results of Near and Far end Coupling for Parallel Microstrip lines in Spacing  $S=3\text{ mm}$

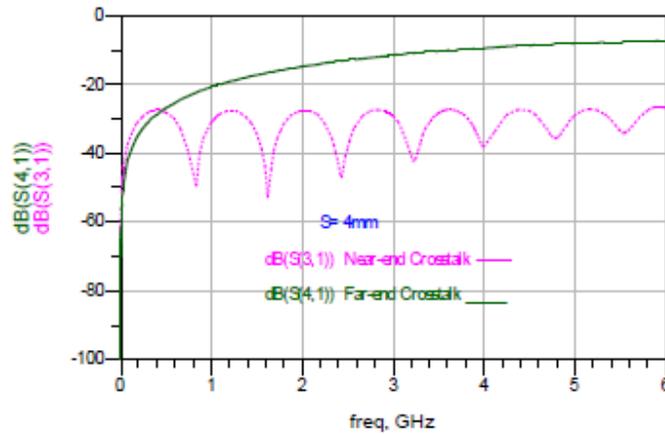


Figure.7. Simulation Results of Near and Far end Coupling for Parallel Microstrip lines in Spacing  $S=4\text{ mm}$

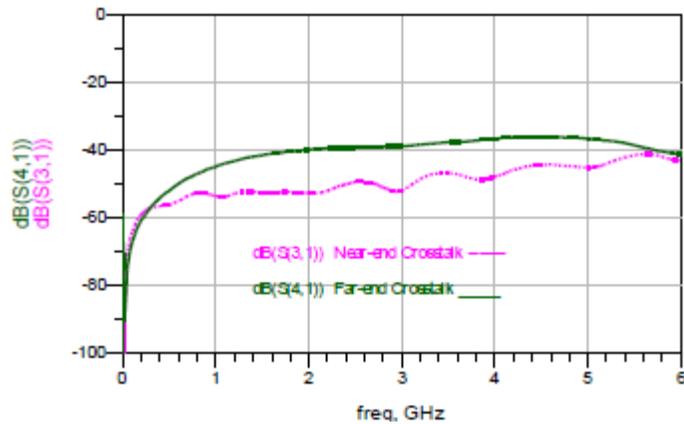


Figure.8. Simulation Results of Near and Far end Coupling for Non Parallel Microstrip lines in Inclination is 300

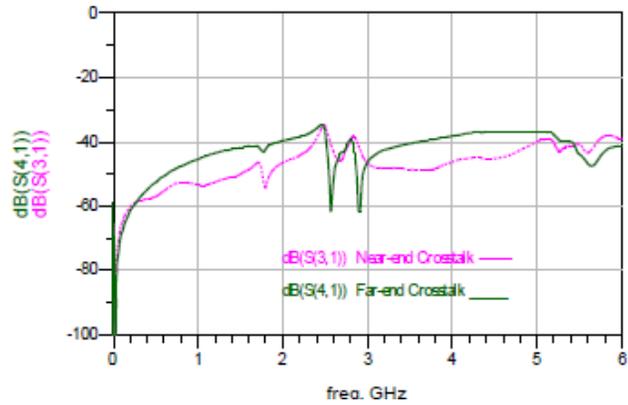


Figure.9. Simulation Results of Near and Far end Coupling for Non-Parallel Microstrip lines with Via fence in Inclination is 300

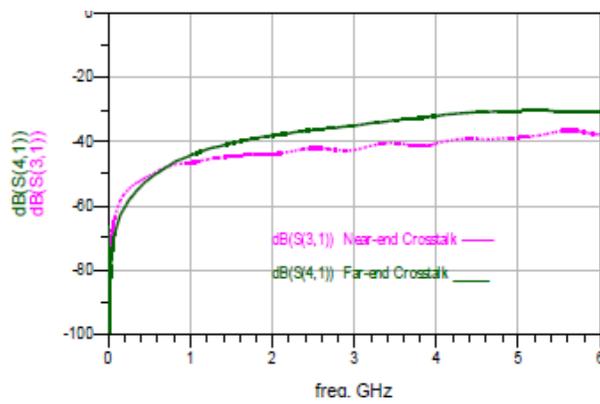


Figure.10. Simulation Results of Near and Far end Coupling for Non Parallel Microstrip lines in Inclination is 450

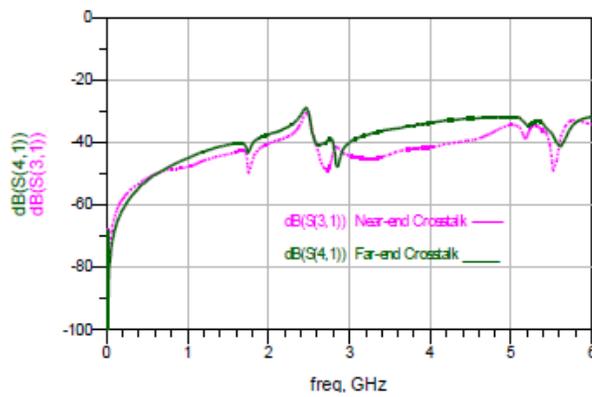


Figure.11. Simulation Results of Near and Far end Coupling for Non Parallel Microstrip lines with Via fence in Inclination is 450

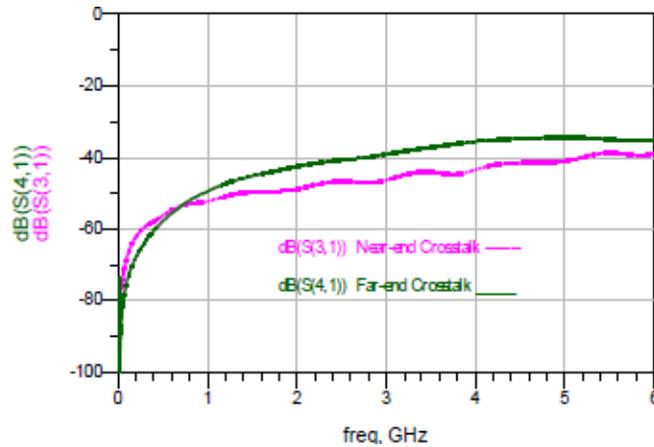


Figure.12. Simulation Results of Near and Far end Coupling for Non Parallel Microstrip lines in Inclination is 600

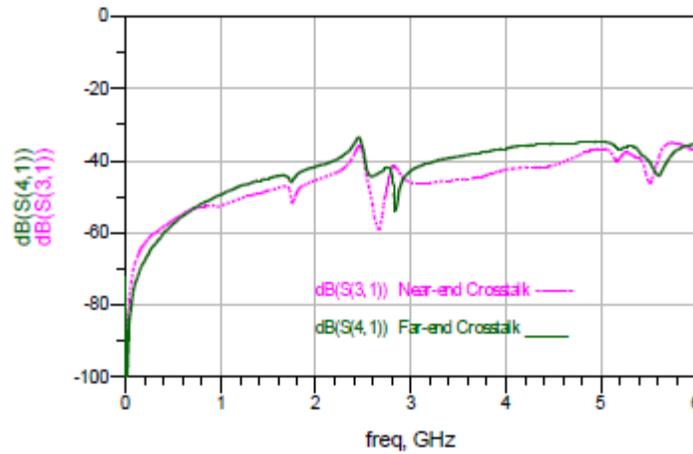


Figure.13. Simulation Results of Near and Far end Coupling for Non Parallel Microstrip lines with Via fence in Inclination is 600

Table 1 summarizes the results of conventional and proposed structures. One way to reduce the far-end coupling is widening the space between aggressor line and victim line. The spacing between two parallel microstrip lines is varied and the near-end and far-end coupling are plotted, which are shown in Fig.5 – Fig.7. We observed that the coupling has been reduced for widening the space between two parallel microstrip lines. Obviously, as the distance between the microstrip lines increases, the coupling decreases monotonically. Hence, if the coupling problems are suspected and the PCB size is not of great concern, maintaining a large enough distance between the lines is none the less an efficient way to reduce the coupling.

Table.1 Comparison of simulated results

Structure		NEXT S(3,1)	FEXT S(4,1)
Parallel Microstrip lines	S=2mm	-26.607dB	-2.541 dB
	S=3mm	-26.312 dB	-5.157 dB
	S=4mm	-26.805 dB	-7.326 dB
Parallel Microstrip lines with Via fence	G=30mm	-14.899 dB	-13.898 dB
Non Parallel Microstrip line	=30 <sup>0</sup>	-43.326 dB	-41.270 dB
	=30 <sup>0</sup> with Via fence	-39.087 dB	-41.270 dB
	=45 <sup>0</sup>	-37.779 dB	-30.884 dB
	=45 <sup>0</sup> with Via fence	-37.102 dB	-35.457 dB
	=60 <sup>0</sup>	-39.060 dB	-35.205 dB
	=60 <sup>0</sup> with Via fence	-37.102 dB	-35.457 dB

Then we have investigated the non-parallel microstripline structures. In this investigation, we compared the results of non-parallel structure with via stitched guard trace. The angle between two non-parallel lines are considered as 30, 45 and 60. When the angle between non-parallel microstrip lines, both near-end and far-end coupling has been reduced. If the angle between two microstrip lines increases, the spacing between two lines are also increases. It occupies more routing space for fabrication. Therefore, for non-parallel microstrip line with 30 angles provides better performance than other angles.

#### 4. CONCLUSIONS

Improving the coupling immunity between adjacent printed circuit board signal traces has become a necessity in modern and highly integrated electronic systems. Conventionally, various structures of signal traces are utilized for this purpose. However, it was shown in this paper that the proper design of these traces is in fact that crucial factor in achieving this goal rather than the mere placement of them between the signal lines. In this paper, we propose a novel design for reducing coupling. We observed NEXT and FEXT for various structures and also for our novel structure.

## REFERENCES

- [1] Fengchao Xiao, Kimitoshi Murano, and yoshio kami. "The Use of via Holes for Controlling the crosstalk of Non Parallel Microstrip lines on PCBs" Proceedings of the IEEE Trans. 2002.
- [2] David A.Hill, fellow, IEEE, Kenneth H.Cavcey, and Robert T.Johnk, Member, IEEE "Crosstalk Between Microstrip Transmission Lines" IEEE Trans. On Electromagnetic Compatibility., Vol36, no 4, PP. 314-321, (November) 1994.
- [3] Y. S. Sohn et al., "Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board," IEEE Trans. Adv. Packag., vol. 24, no. 4, pp. 521–527, (November). 2001.
- [4] T. H. Kim et al., "Signal transient and crosstalk model of capacitively and inductively coupled VLSI interconnect lines," J. Semiconductor Technol. Sci., vol. 7, no. 4, pp. 260–266, (December). 2007.
- [5] S. K. Lee et al., "FEXT-eliminated stub-alternated microstrip line for multi-gigabit/second parallel links," Electron. Lett., vol. 44, no. 4, pp. 272–273, (February). 2008.
- [6] L. Zhi, W. Qiang, and S. Changsheng, "Application of guard traces with vias in the RF PCB layout," in Proc. 3rd Int. Symp. Electromagn. Compatibil., Beijing, China, (May) 2002, pp. 771–774.
- [7] E. Bogatin, Signal Integrity Simplified. Upper Saddle River, NJ:Prentice Hall, 2004, p. 304.
- [8] J. F. Buckwalter et al., "Cancellation of crosstalk-induced jitter," IEEE J. Solid State Circuits, vol. 41, no. 3, pp. 621–632, (March). 2006.
- [9] K. Lee et al., "Reduction of transient far-end crosstalk voltage and jitter in DIMM connectors for DRAM interface," IEEE Microwave Wireless Compon. Lett., vol. 19, pp. 15–17, (January). 2009.
- [10] Howard W. Johnson, High-speed digital design: a Englewood Cliffs, N.J. : handbook of black magic. Prentice Hall, 1993.

## Authors

**Mr.M.Anandan**, Associate Professor of Electronics and Communication Engineering at Latha Mathavan Engineering College, Alagarkovil Madurai .He obtained his B.E (ECE) degree from Madurai Kamaraj University, Madurai in 1996 and M.E. (Communication Systems) degree from Anna University, Chennai in 2008. He has 9 years of Industrial Experience and 4.5 years of Teaching Experience. He has published one National journal and two papers in National conferences



**Dr. N.Suresh Kumar**, Professor and Principal of Velammal College of Engineering & Technology, Madurai, obtained his B.E., M.E. and Ph.D degree from Madurai Kamaraj University, Madurai. He has 25 years of Teaching, Administration and Research experience. He has co-authored 8 books, published and presented many research papers in journals and international conferences. His area of research includes EMI/EMC and Optical communication. .He is a Recipient of Second Best Paper award in INCEMIC2006.



**Mrs.P.Rajeswari**, Assistant Professor of ECE Department of Velammal College of Engineering & Technology, Madurai, obtained her B.E., degree from Madurai Kamaraj University, Madurai and M.E. degree from Anna University, Chennai. She has more than 13 years of Teaching experience. Pursuing Ph.D. in Anna University, Tirunelveli in EMI/EMC. She published and presented many research papers in journals and international conferences. Her area of research includes EMI/EMC and Wireless communication. She is Life member of ISTE, IETE and Society of EMC Engineers (India).



**A.GOBINATH**, Junior Research Fellow of Velammal College of Engineering & Technology, Madurai, obtained his B.E. from Anna university of Technology, Tirunelveli. He is doing research in the area of EMI/EMC. He has 2.5 year research experience. He published paper in international conference.