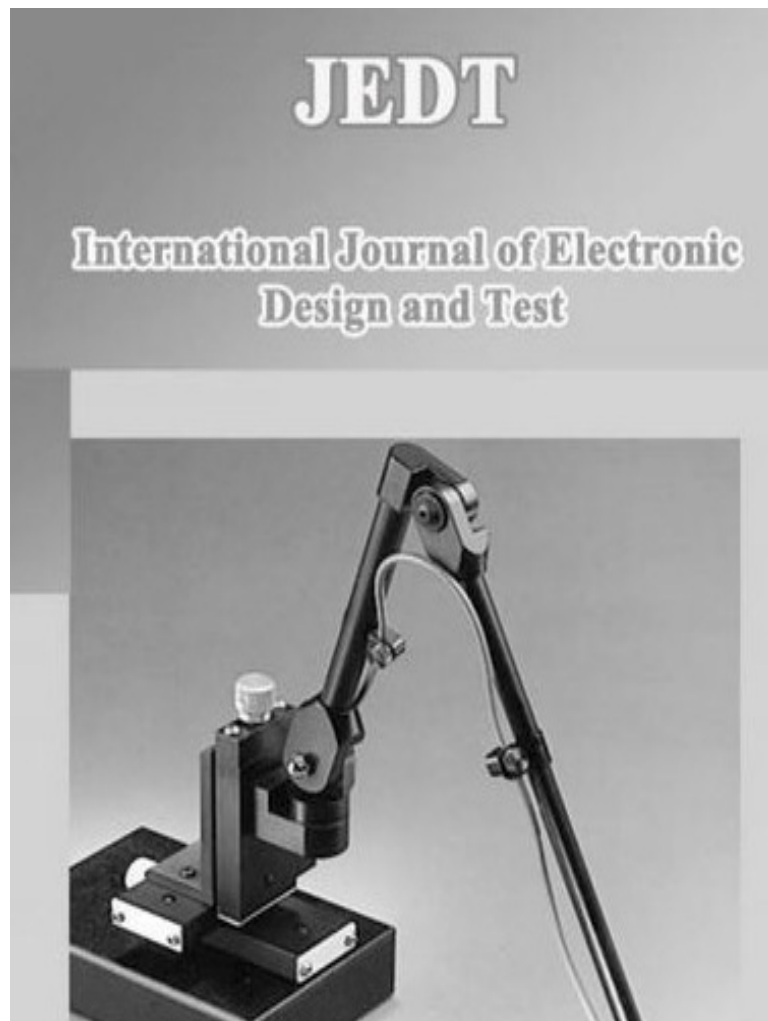


International Journal of Electronic Design and Test(JEDT)



<http://airccse.com/jedt/index.html>

Scope of the journal

International Journal of Electronic Design and Test(JEDT) is a peer-reviewed, open access journal which invites original works describing the methods used to design and test electronic product hardware and supportive software. Authors from industry and academia are invited to submit their original unpublished research works on the topics listed below:

Topics of interest

- Passive components (filters, couplers, transitions, etc)
- IC/module design
- Low-power design
- Electronic design automation
- Design/test verification
- Fault modelling
- Test generation
- Fault simulation
- Design of testability
- Synthesis of testability
- Built-in self-test
- Test specifications
- Formal verification of hardware
- Simulation for verification
- Design debugging
- Testing of VLSI devices printed circuit boards, and electronic systems
- Testing of analog and digital electronic circuits
- Testing of microprocessors, memories and signal processing devices
- SOC and SIP testing
- Memory and FPGA test and repair
- Delay testing
- IDDQ test
- Novel test methods
- Effectiveness of test methods
- Fault models and ATPG, and DPPM prediction
- DFT for analog/mixed signal ICs and system-on-chip
- DFT and BIST for digital and SoC

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All manuscripts will be subject to a well established, fair, unbiased peer review and refereeing procedure, and are considered on the basis of their significance, novelty and usefulness to the Journals readership. The reviewing structure will always ensure the anonymity of the referees & it will be reviewed by 3 experts in the field. The review output will be one of the following decisions:

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2. Accept with minor changes
3. Weak Accept with major changes
4. Reject

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